AMENDMENT

(amendment under the provision of Article 11)

To : The Commissioner of Patent Office Esq.

1 . Indication of International Application : PCT/JP03/07676

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4. Object of the Amendment

claims

5. Contents of the Amendment

(1) To delete claim 1 (on page 33) to claim 35 (on page 39)

(2) To add claim 36 (on page 39/1) to claim 89 (on 39/10)

6. List of the Attachments

Claims (pages 33 to 39) and claims (on pages 39/1 39/10)

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36. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:
said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer, a second metal layer is in contact with said first metal layer, and a third layer is in contact with said second layer;
said second metal layer comprises a metal material having a higher melting point than those of the metal materials in said first metal layer and said third metal layer;
said third metal layer comprises a metal material having a lower resistivity than those of the metal materials in said first metal layer and said second metal layer;
said first metal layer comprises any metal material selected from a group comprising Ni, Pt, Pd, Ni_zSi_{1-z}, Pt_zSi_{1-z}, Pd_zSi_{1-z}, Ni_zN_{1-z}, and Pd_zN_{1-z} (where, $0<z<1$); and
said second metal layer comprises any metal material selected from a group comprising Mo, W, Ta, Mo_xSi_{1-x}, Pt_xSi_{1-x}, W_xSi_{1-x}, Ti_xSi_{1-x}, Ta_xSi_{1-x}, Mo_xN_{1-x}, W_xN_{1-x}, Ti_xN_{1-x}, and Ta_xN_{1-x} (where, $0<x<1$).

37. A semiconductor device according to claim 36, wherein said third metal layer comprises any metal material selected from a group comprising Au, Cu, Al、 and Pt.

38. A semiconductor device according to claim 36, wherein said first metal material comprises a metal material having a higher work function than that of the metal material in said second metal material.

39. A semiconductor device according to claim 38, wherein said metal layer comprises a metal material having a higher work function than that of the metal material in said third metal layer.

40. A semiconductor device according to claim 36, wherein the melting point of said second metal layer is 1,000°C or higher.

41. A semiconductor device according to claim 36, wherein said semiconductor layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

42. A semiconductor device according to claim 41, wherein said substrate comprises any substrate selected from a group comprising a sapphire substrate, a SiC substrate, and a GaN substrate.

43. A semiconductor device according to claim 36, wherein said semiconductor layer

is an $Al_uGa_{1-u}N$ layer (where, $0 \leqq u \leqq 1$).

44. A semiconductor device according to claim 36, wherein said semiconductor layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

45. A semiconductor device according to claim 44, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and a GaN compound semiconductor electron supplying layer comprises AlGaN.

46. A semiconductor device according to claim 36, wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

47. A semiconductor device according to claim 46, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

48. A semiconductor device according to claim 36, wherein said semiconductor layer is a n-type GaN channel layer.

49. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer, a second metal layer is in contact with said first metal layer, and a third layer is in contact with said second layer;

said second metal layer comprises a metal material having a higher melting point than those of the metal materials in said first metal layer and said third metal layer;

said third metal layer comprises a metal material having a lower resistivity than those of the metal materials in said first metal layer and said second metal layer;

said first metal layer comprises any metal material selected from a group comprising $Ni_{z1}Si_{1-z1}$ (where, $0.4 \leqq z1 \leqq 0.75$), $Pt_{z2}Si_{1-z2}$ (where, $0.5 \leqq z2 \leqq 0.75$), $Pd_{z3}Si_{1-z3}$ (where, $0.5 \leqq z3 \leqq 0.85$), $Ni_{z4}N_{1-z4}$ (where, $0.5 \leqq z4 \leqq 0.85$), and $Pd_{z5}N_{1-z5}$ (where, $0.5 \leqq z5 \leqq 0.85$); and

said second metal layer comprises any metal material selected from a group comprising Mo, W, Ta, Mo_xSi_{1-x}, Pt_xSi_{1-x}, W_xSi_{1-x}, Ti_xSi_{1-x}, Ta_xSi_{1-x}, Mo_xN_{1-x}, W_xN_{1-x},

Ti_xN_{1-x}, and Ta_xN_{1-x} (where, $0<x<1$).

50. A semiconductor device according to claim 49, wherein said third metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

51. A semiconductor device according to claim 49, wherein said first metal layer comprises a metal material having a higher work function than that of the metal material in said second metal layer.

52. A semiconductor device according to claim 51, wherein said first metal layer comprises a metal material having a higher work function than that of the metal material in said third metal layer.

53. A semiconductor device according to claim 49, wherein the melting point of said second metal layer is 1,000°C or higher.

54. A semiconductor device according to claim 49, wherein said semiconductor layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

55. A semiconductor device according to claim 54, wherein said substrate comprises any substrate selected from a group comprising a sapphire substrate, a SiC substrate and a GaN substrate.

56. A semiconductor device according to claim 49, wherein said semiconductor layer is an $Al_uGa_{1-u}N$ layer (where, $0 \leqq u \leqq 1$).

57. A semiconductor device according to claim 49, wherein said semiconductor layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

58. A semiconductor device according to claim 57, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and GaN compound semiconductor electron supplying layer comprises AlGaN.

59. A semiconductor device according to claim 49, wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

60. A semiconductor device according to claim 59, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

61. A semiconductor device according to claim 49, wherein said semiconductor layer is a n-type GaN channel layer.

62. A semiconductor device comprising a semiconductor layer comprising a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer;

said first metal layer comprises a metal material having a higher meting point than that of the metal material in said second metal layer;

said second metal layer comprises a metal material having a lower resistivity than that of the metal material in said first metal layer: and

said first metal layer comprises any metal material selected from a group comprising Ni_yN_{1-y} and Pd_yN_{1-y} (where, $0<y<1$).

63. A semiconductor device according to claim 62, wherein said second metal layer comprises any metal material selected from a group comprising any metal material selected from a group comprising Au, Cu, Al, and Pt.

64. A semiconductor device according to claim 62, wherein said first metal layer has a higher work function than said second metal layer.

65. A semiconductor device according to claim 62, wherein the melting point of said first metal layer is 1,000°C or higher.

66. A semiconductor device according to claim 62, wherein said semiconductor layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

67. A semiconductor device according to claim 66, wherein said substrate comprises any substrate selected from a group a sapphire substrate, a SiC substrate, and a GaN substrate.

68. A semiconductor device according to claim 62, wherein said semiconductor layer is an $Al_uGa_{1-u}N$ layer (where, $0 \leqq u \leqq 1$).

69. A semiconductor device according to claim 62, wherein said semiconductor layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

70. A semiconductor device according to claim 69, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and GaN compound semiconductor electron supplying layer comprises AlGaN.

71. A semiconductor device according to claim 62, wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

72. A semiconductor device according to claim 71, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

73. A semiconductor device according to claim 62, wherein said semiconductor layer is a n-type GaN channel layer.

74. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer;

said first metal layer comprises a metal material having a higher meting point than that of the metal material in said second metal layer;

said second metal layer comprises a metal material having a lower resistivity than that of the metal material of said first metal layer: and

said first metal layer comprises any metal material selected from a group comprising $Ni_{y4}N_{1-y4}$ and $Pd_{y5}N_{1-y5}$ (where, $0.5 \leqq y5 \leqq 0.85$).

75. A semiconductor device according to claim 74, wherein said second metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

76. A semiconductor device according to claim 74, wherein said first metal layer has a higher work function than said second metal layer.

77. A semiconductor device according to claim 74, wherein the melting point of said first metal layer is 1,000°C or higher.

78. A semiconductor device according to claim 74, wherein said semiconductor layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

79. A semiconductor device according to claim 78, wherein said substrate comprises any substrate selected from a group comprising a sapphire substrate, a SiC substrate, and a GaN substrate.

80. A semiconductor device according to claim 74, wherein said semiconductor layer is an $Al_uGa_{1-u}N$ layer (where, $0 \leqq u \leqq 1$).

81. A semiconductor device according to claim 74, wherein said semiconductor layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

82. A semiconductor device according to claim 81, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

83. A semiconductor device according to claim 74, wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

84. A semiconductor device according to claim 83, wherein said GaN semiconductor channel layer comprises a compound semiconductor selected from GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

85. A semiconductor device according to claim 74, wherein said semiconductor layer is a n-type GaN channel layer.

86. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of the

Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer, a second metal layer is in contact with said first metal layer, and a third layer is in contact with said second layer;

said first metal layer comprises any metal material selected from a group comprising Ni, Pt, Pd, Ni_zSi_{1-z}, Pt_zSi_{1-z}, Pd_zSi_{1-z}, Ni_zN_{1-z}, and Pd_zN_{1-z} (where, $0<z<1$);

said second metal layer comprises any metal material selected from a group comprising Mo, W, Ta, Mo_xSi_{1-x}, Pt_xSi_{1-x}, W_xSi_{1-x}, Ti_xSi_{1-x}, Ta_xSi_{1-x}, Mo_xN_{1-x}, W_xN_{1-x}, Ti_xN_{1-x} and Ta_xN_{1-x} (where, $0<x<1$);

said third metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

87. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer;

said first metal layer comprises any metal material selected from a group comprising Ni_yN_{1-y} and Pd_yN_{1-y} (where, $0<y<1$); and

said second metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

88. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer, a second metal layer is in contact with said first metal layer and a third metal layer is in contact with said second metal layer;

said first metal layer comprises any metal material selected from a group comprising $Ni_{z1}Si_{1-z1}$ (where, $0.4 \leqq z1 \leqq 0.75$), $Pt_{z2}Si_{1-z2}$ (where, $0.5 \leqq z2 \leqq 0.75$), $Pd_{z3}Si_{1-z3}$ (where, $0.5 \leqq z3 \leqq 0.85$), $Ni_{z4}N_{1-z4}$ (where, $0.5 \leqq z4 \leqq 0.85$), and $Pd_{z5}N_{1-z5}$ (where, $0.5 \leqq z5 \leqq 0.85$);

said second metal layer comprises any metal material selected from a group comprising Mo, W, Ta, Mo_xSi_{1-x}, Pt_xSi_{1-x}, W_xSi_{1-x}, Ti_xSi_{1-x}, Ta_xSi_{1-x}, Mo_xN_{1-x}, W_xN_{1-x}, Ti_xN_{1-x}, and Ta_xN_{1-x} (where, $0<x<1$); and

said third metal layer comprises any metal material selected from a group

comprising Au, Cu, Al, and Pt.

89. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leqq v \leqq 1$) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer;

said first metal layer comprises any metal material selected from a group comprising $Ni_{y4}N_{1-y4}$ (where, $0.5 \leqq y4 \leqq 0.85$) and $Pd_{y5}N_{1-y5}$ (where, $0.5 \leqq y5 \leqq 0.85$); and

said second metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.